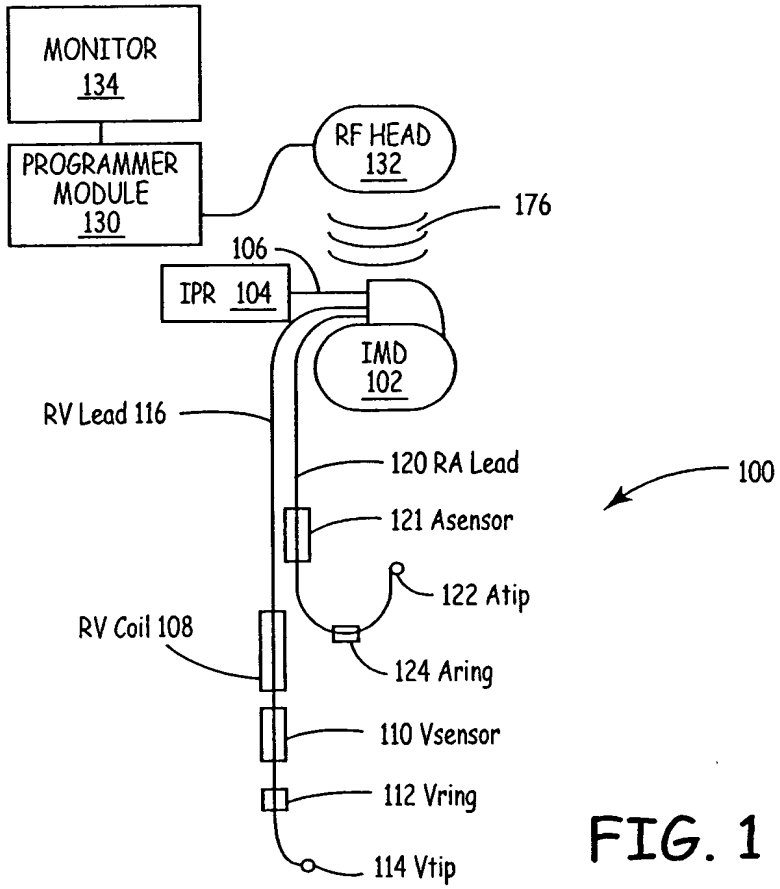

MONITOR
134
PROGRAMMER MODULE
130
RF HEAD
132
176
106
IPR 104
IMD
102
RV Lead 116
120 RA Lead
100
121 Asensor
122 Atip
RV Coil 108
124 Aring
110 Vsensor
112 Vring
114 Vtip

FIG. 1

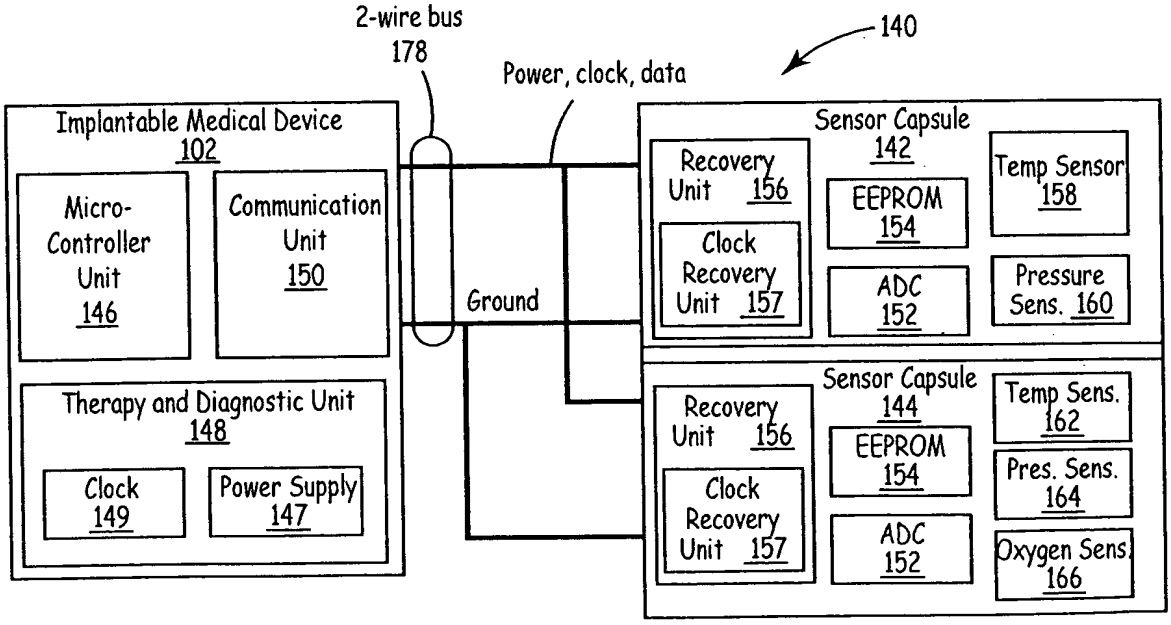

2-wire bus
178
Power, clock, data
140
Implantable Medical Device
102
Micro-Controller Unit
146
Communication Unit
150
Therapy and Diagnostic Unit
148
Clock
149
Power Supply
147
Ground
Sensor Capsule
142
Recovery Unit 156
Clock Recovery Unit 157
EEPROM
154
ADC
152
Temp Sensor
158
Pressure Sens. 160
Sensor Capsule
144
Recovery Unit 156
Clock Recovery Unit 157
EEPROM
154
ADC
152
Temp Sens.
162
Pres. Sens.
164
Oxygen Sens.
166

FIG. 2

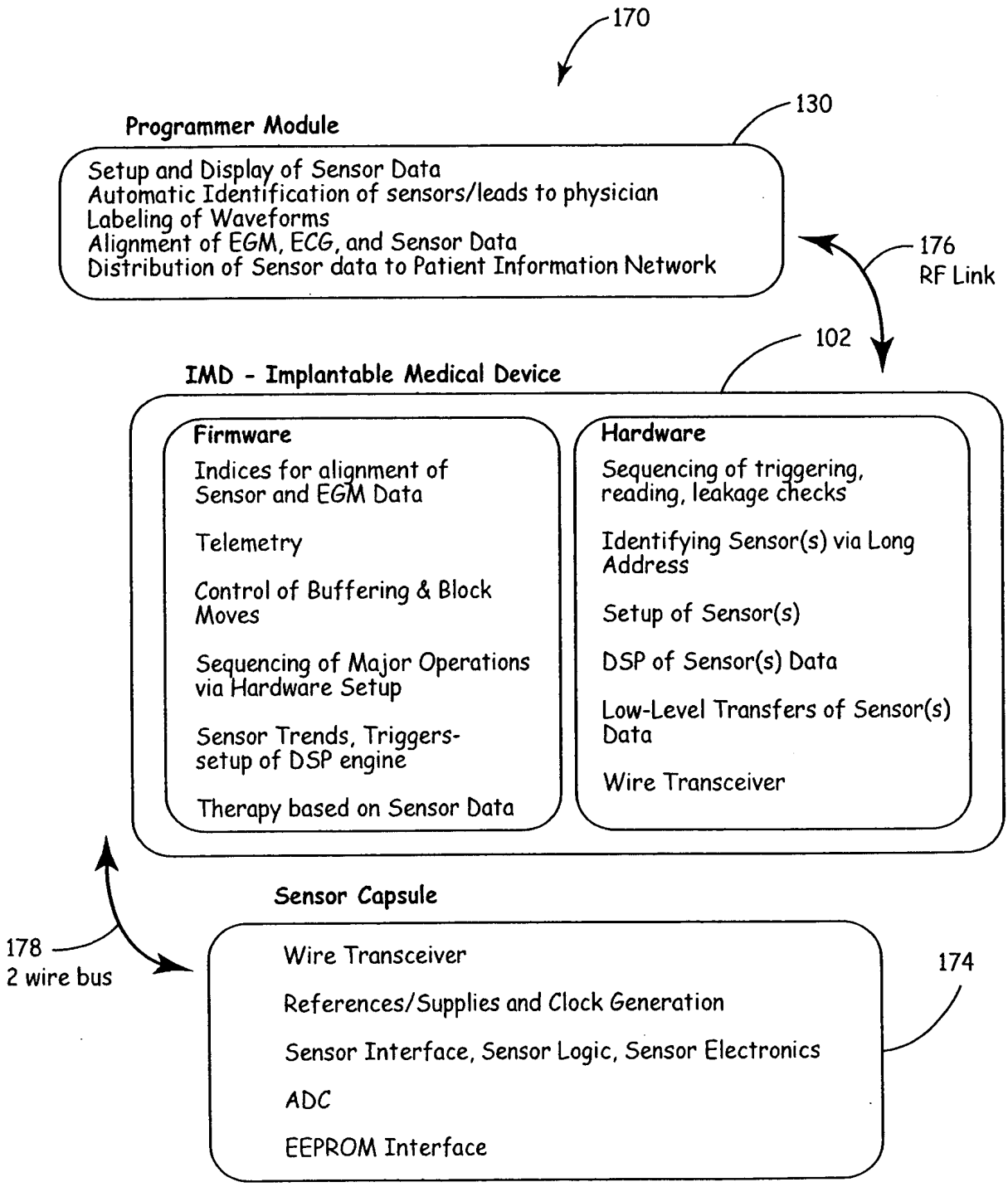

170
Programmer Module
130
Setup and Display of Sensor Data
Automatic Identification of sensors/leads to physician
Labeling of Waveforms
Alignment of EGM, ECG, and Sensor Data
Distribution of Sensor data to Patient Information Network
176
RF Link
102
IMD - Implantable Medical Device
Firmware
Indices for alignment of Sensor and EGM Data
Telemetry
Control of Buffering & Block Moves
Sequencing of Major Operations via Hardware Setup
Sensor Trends, Triggers-setup of DSP engine
Therapy based on Sensor Data
Hardware
Sequencing of triggering, reading, leakage checks
Identifying Sensor(s) via Long Address
Setup of Sensor(s)
DSP of Sensor(s) Data
Low-Level Transfers of Sensor(s) Data
Wire Transceiver
178
2 wire bus
Sensor Capsule
Wire Transceiver
References/Supplies and Clock Generation
Sensor Interface, Sensor Logic, Sensor Electronics
ADC
EEPROM Interface
174

FIG. 3

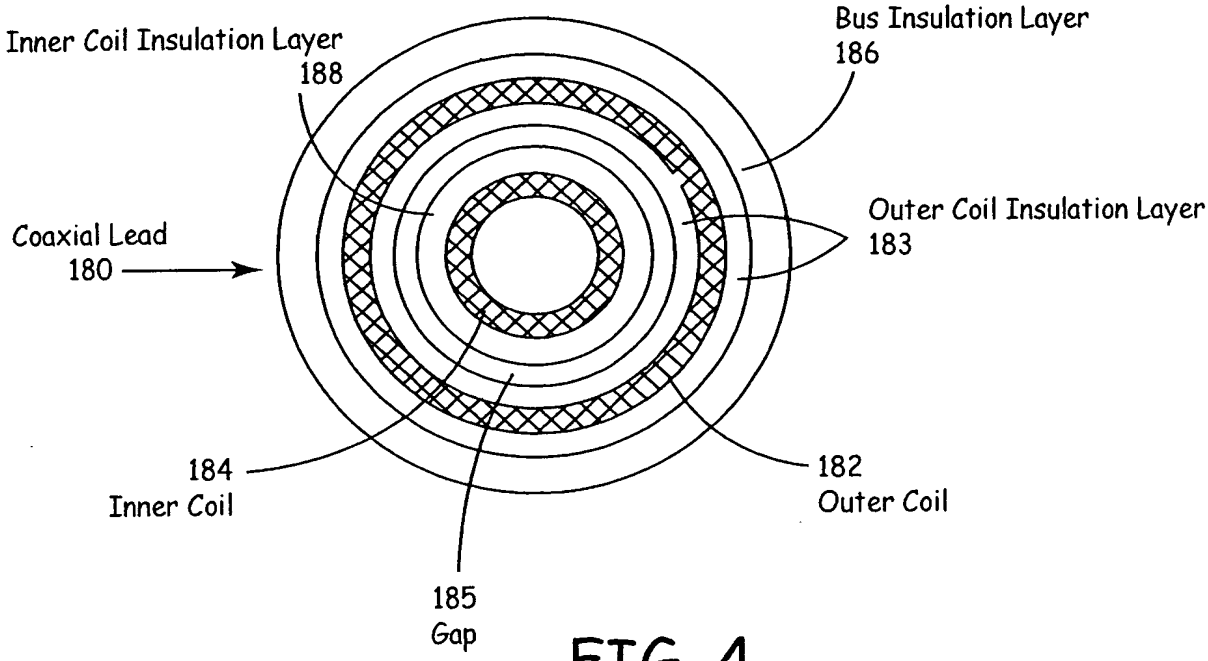

Inner Coil Insulation Layer
188
Bus Insulation Layer
186
Coaxial Lead
180
Outer Coil Insulation Layer
183
184
Inner Coil
182
Outer Coil
185
Gap

FIG. 4

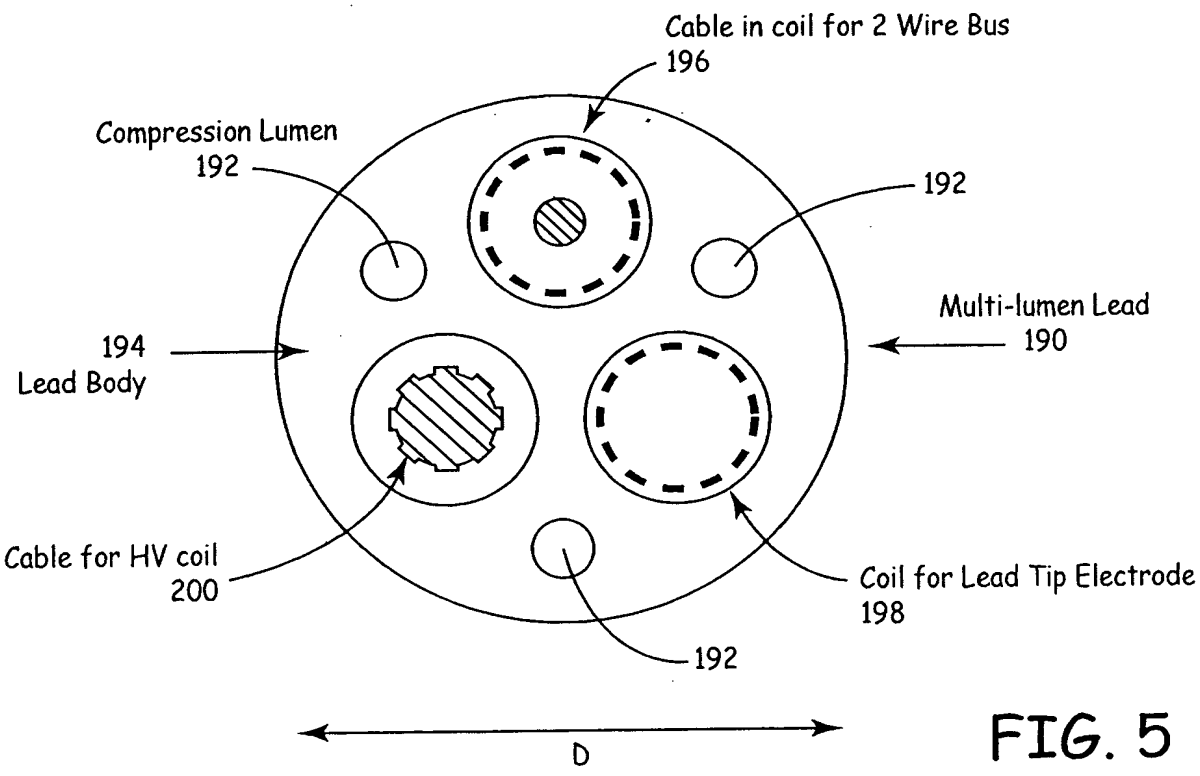

Cable in coil for 2 Wire Bus
196
Compression Lumen
192
192
Multi-lumen Lead
190
194
Lead Body
Cable for HV coil
200
Coil for Lead Tip Electrode
198
192
D

FIG. 5

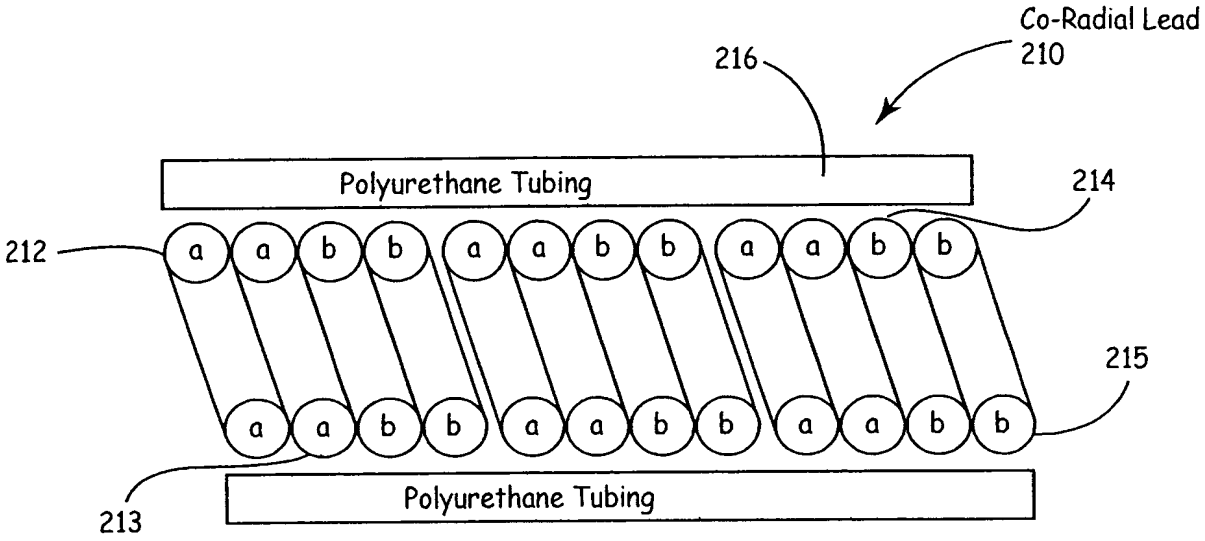

Co-Radial Lead
210
216
Polyurethane Tubing
214
212
a a b b a a b b a a b b
215
a a b b a a b b a a b b
213
Polyurethane Tubing

FIG. 6

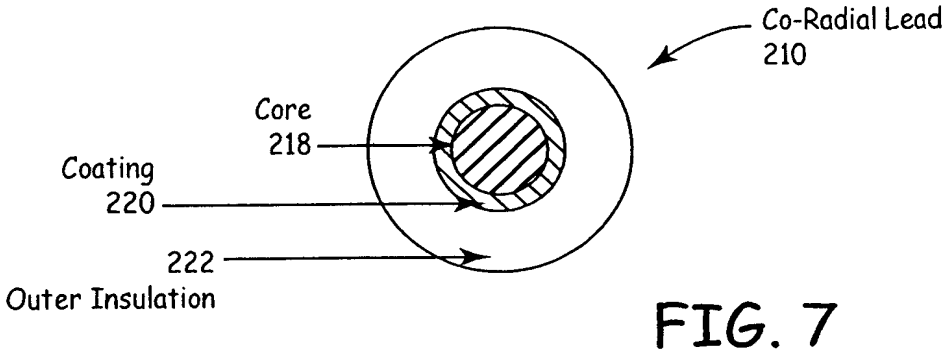

Co-Radial Lead
210
Core
218
Coating
220
222
Outer Insulation

FIG. 7

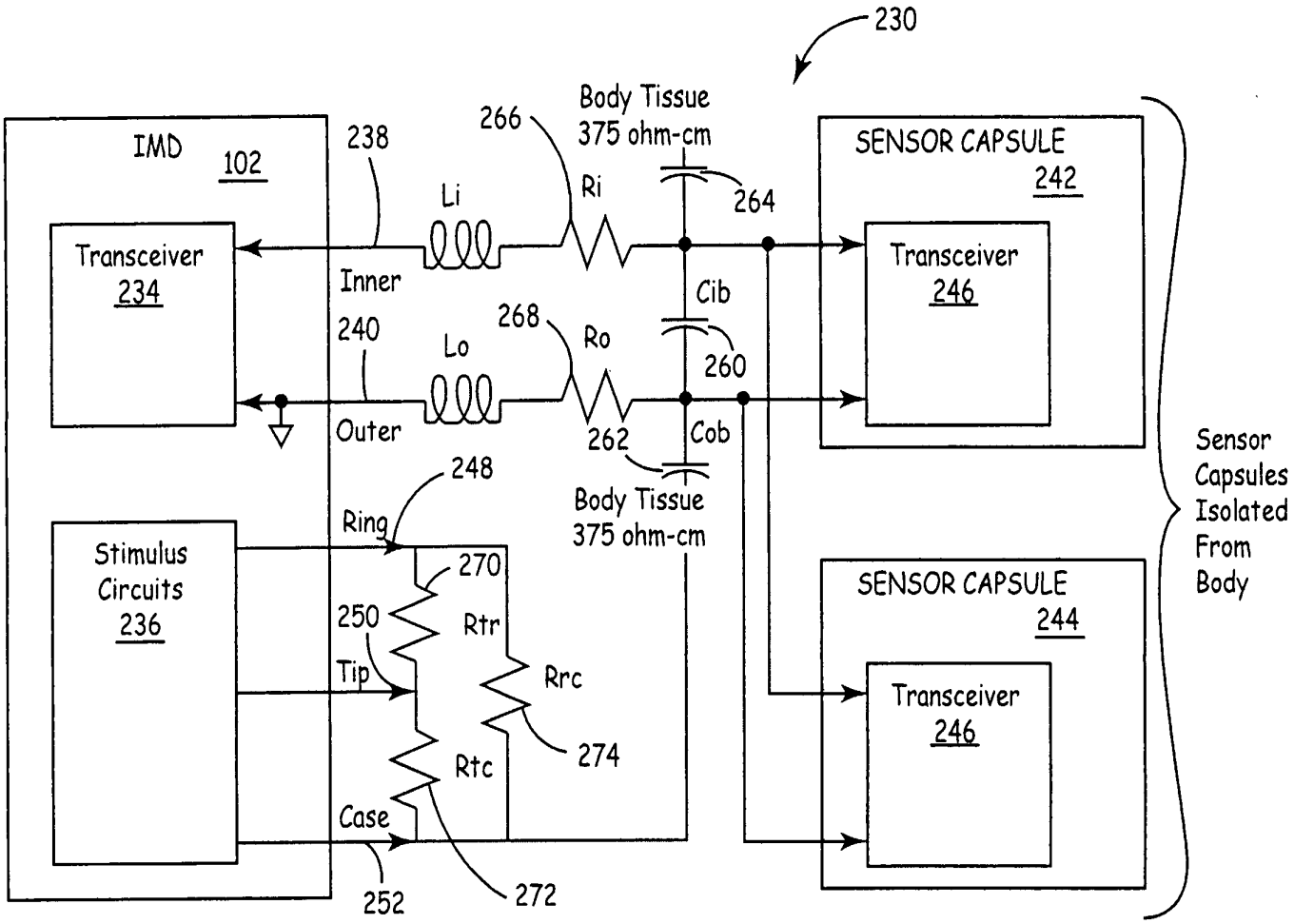

230
IMD
102
238
266
Body Tissue
375 ohm-cm
SENSOR CAPSULE
242
Li
Ri
264
Transceiver
234
Inner
Transceiver
246
Cib
240
268
Lo
Ro
260
Outer
262
Cob
248
Body Tissue
375 ohm-cm
Ring
Sensor
Capsules
Isolated
From
Body
Stimulus
Circuits
236
270
SENSOR CAPSULE
244
250
Rtr
Tip
Rrc
Transceiver
246
274
Rtc
Case
252
272

FIG. 8

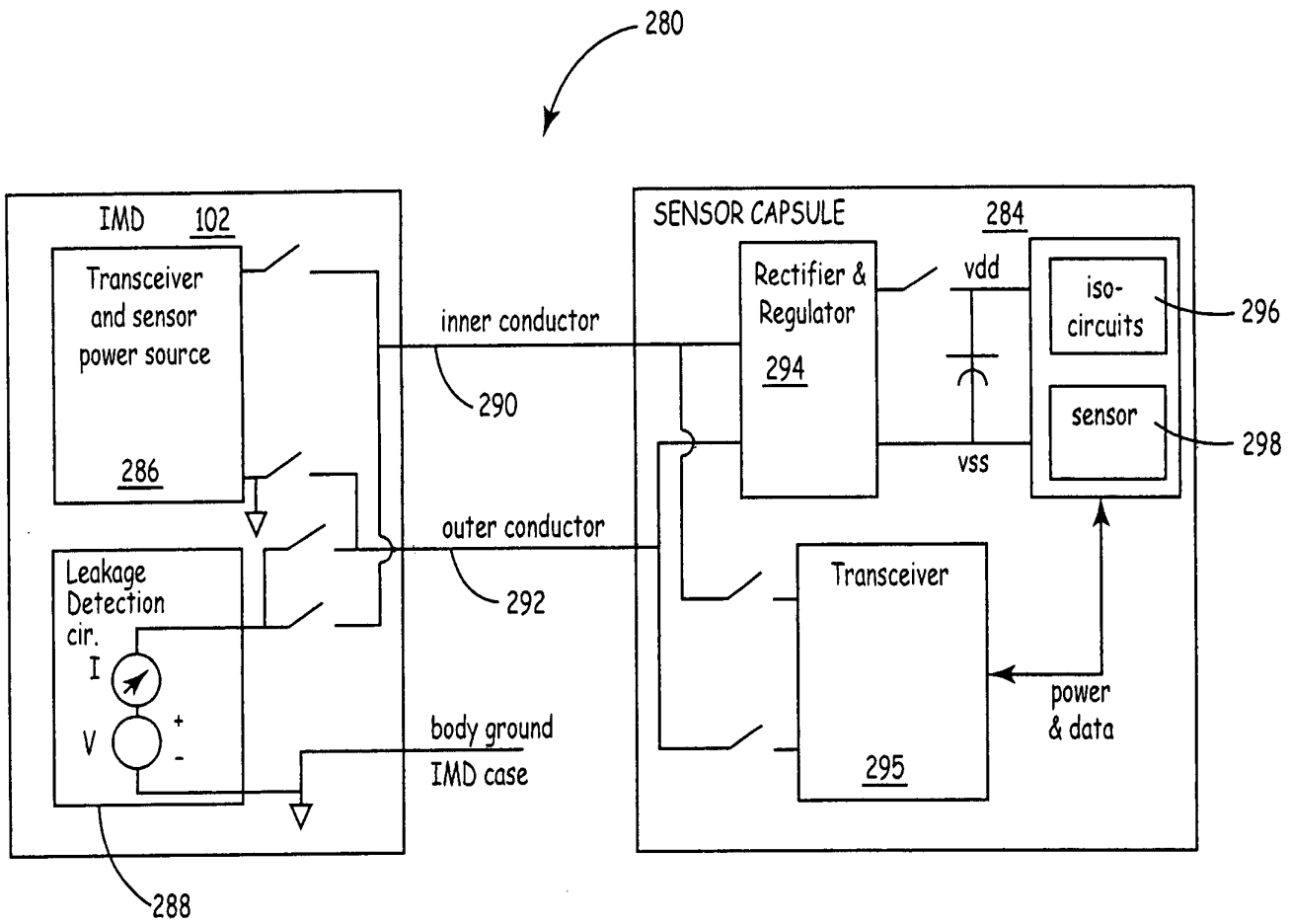
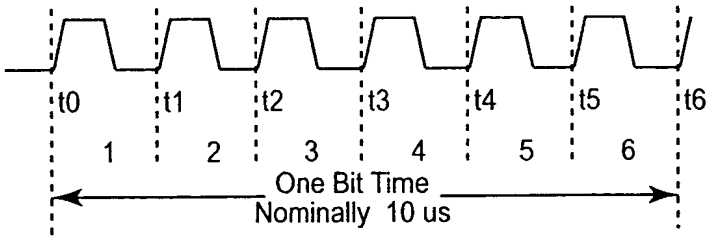
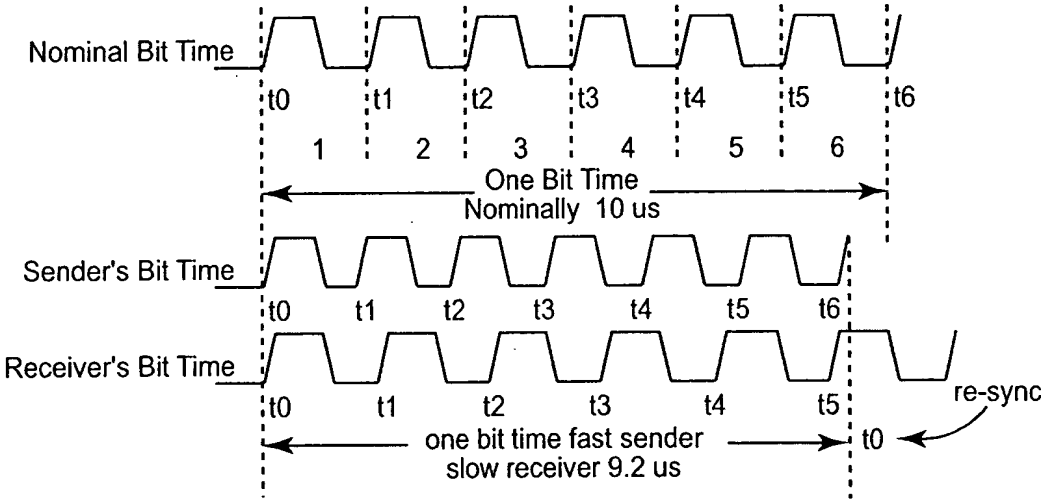

280
IMD 102
Transceiver and sensor power source
286
Leakage Detection cir.
I
V
+
-
288
inner conductor
290
outer conductor
292
body ground
IMD case
SENSOR CAPSULE 284
Rectifier & Regulator
294
vdd
vss
iso-circuits
296
sensor
298
Transceiver
295
power & data

FIG. 9



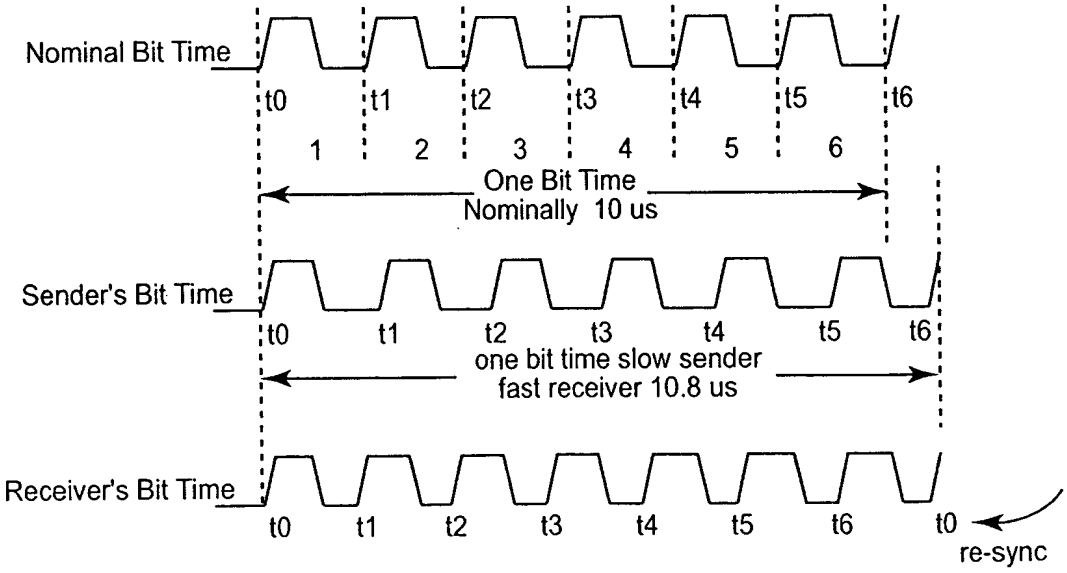
Nominally One Bit Time

FIG. 10



Fast Sender - Slow Receiver One Bit Time

FIG. 11



Slow Sender - Fast Receiver One Bit Time

FIG. 12

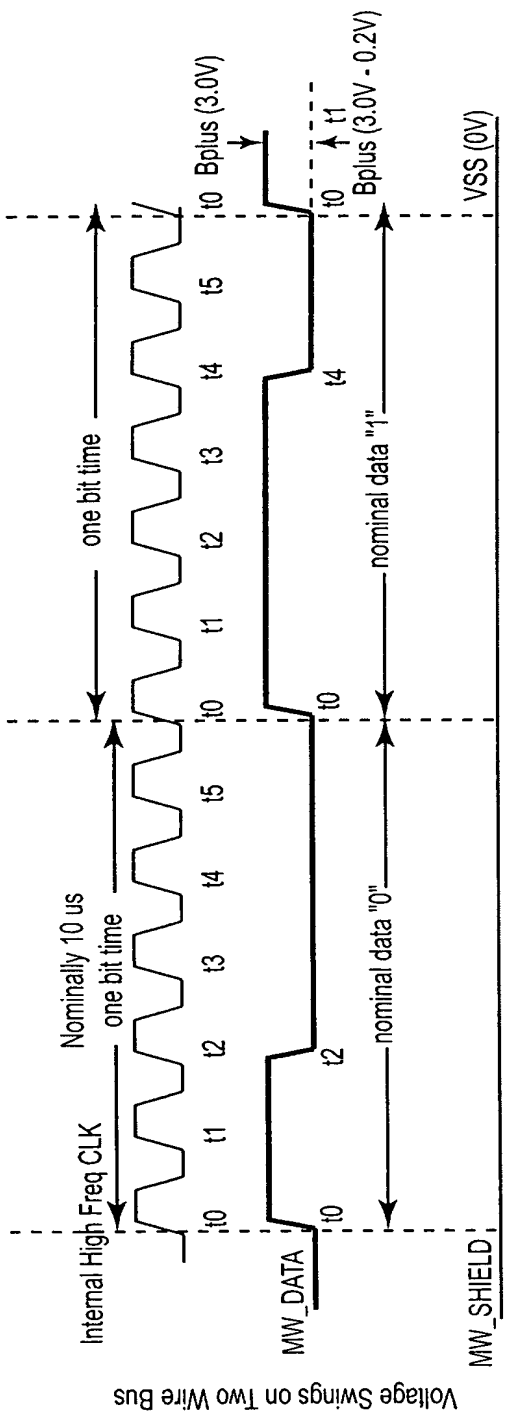

Voltage Swings on Two Wire Bus
Internal High Freq CLK
Nominally 10 us
one bit time
one bit time
MW_DATA
MW_SHIELD
t0
t1
t2
t3
t4
t5
nominal data "0"
nominal data "1"
Bplus (3.0V)
Bplus (3.0V - 0.2V)
VSS (0V)

FIG. 13

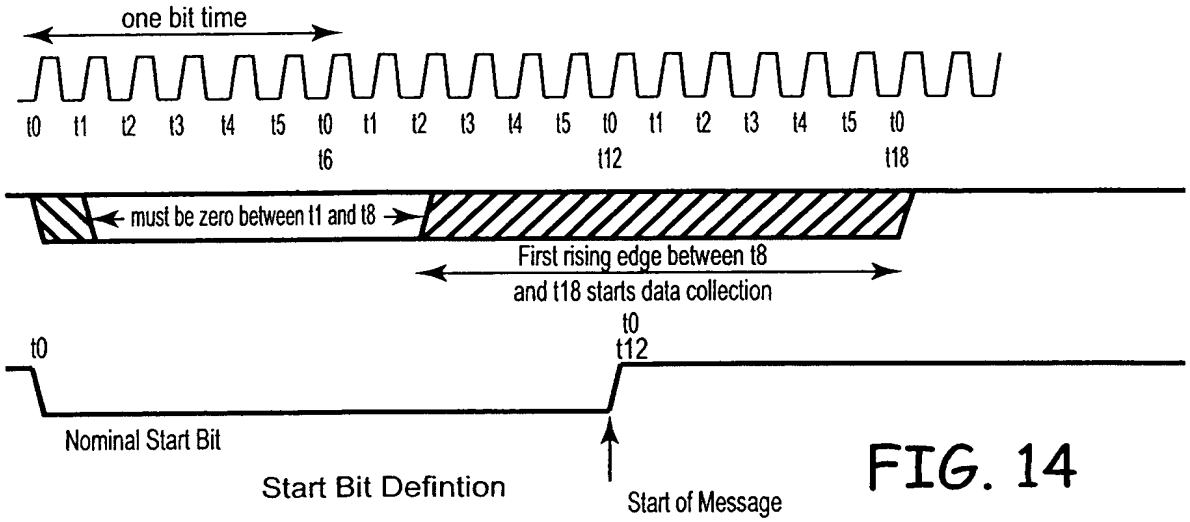


FIG. 14

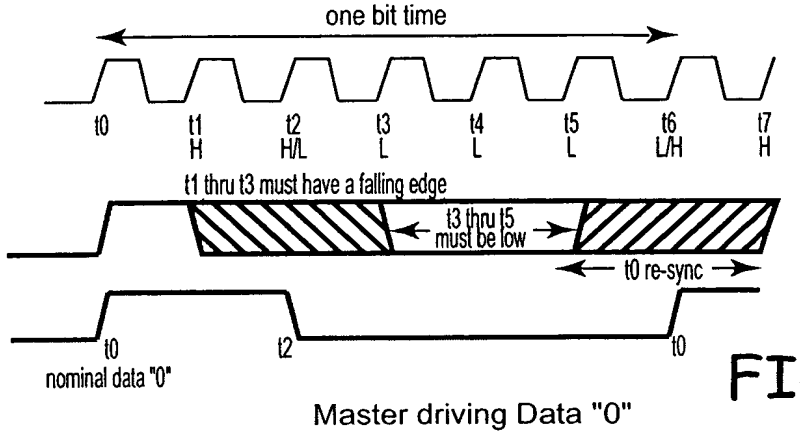


FIG. 15

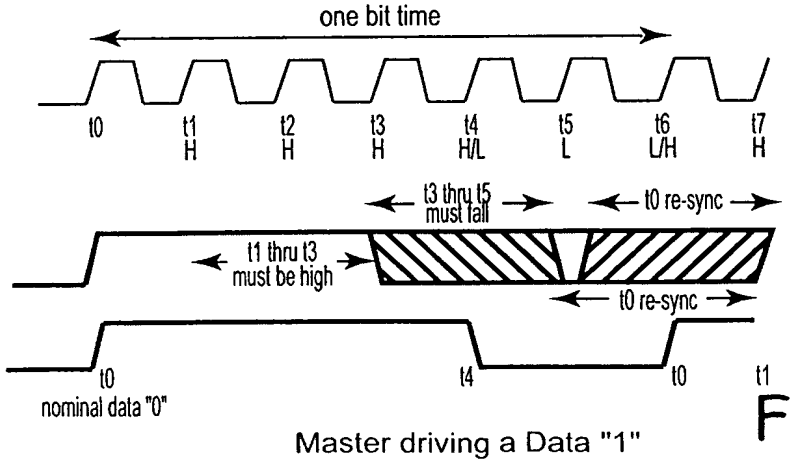


FIG. 16

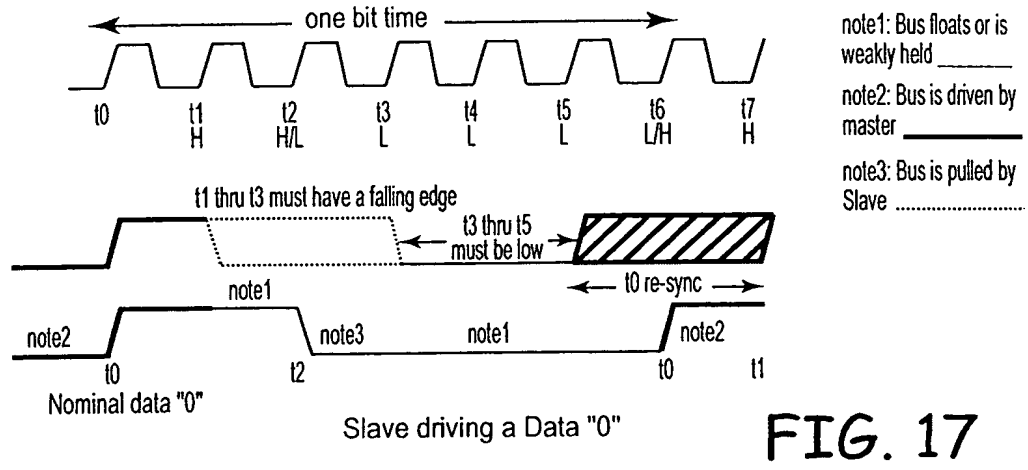


FIG. 17

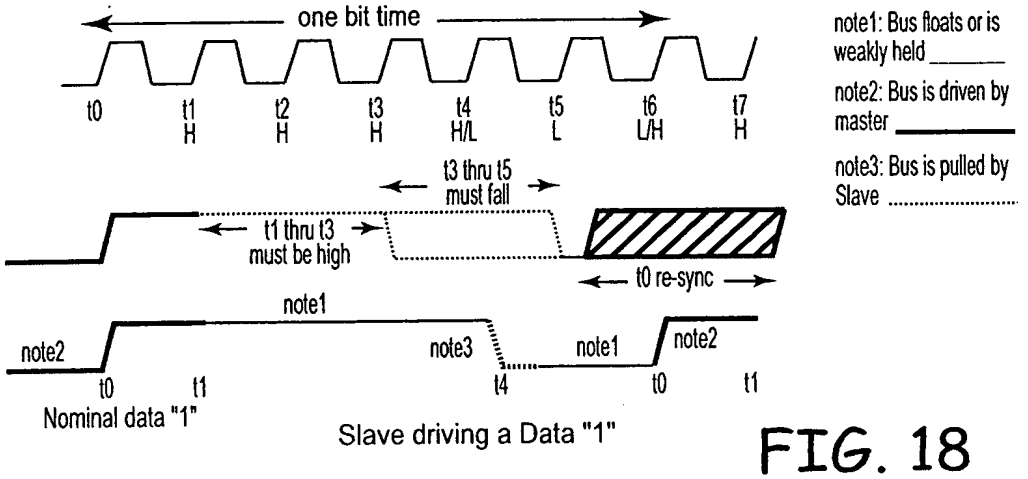


FIG. 18

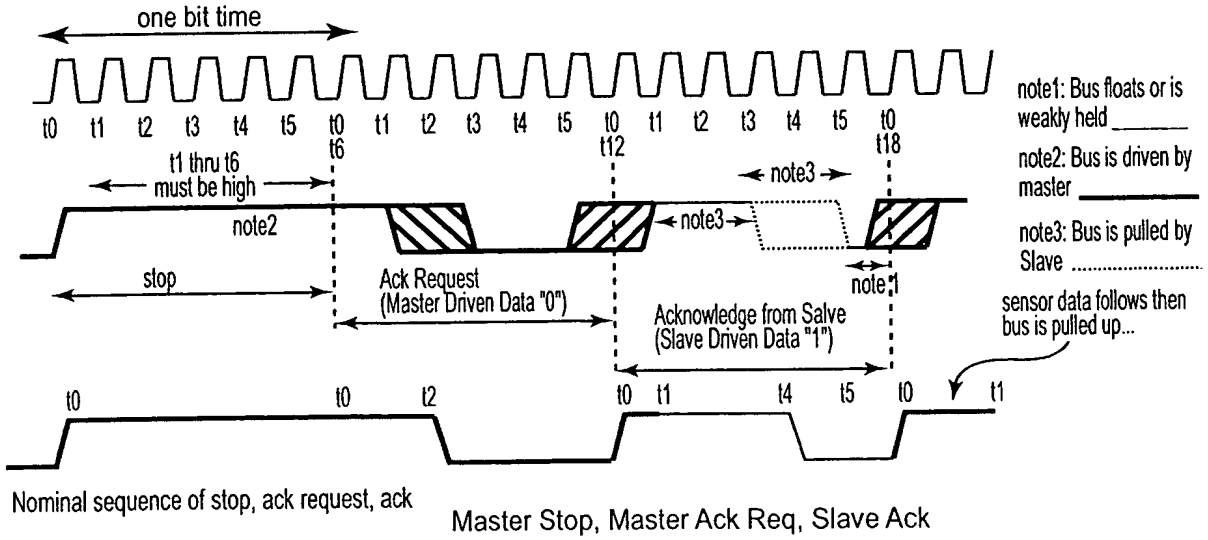
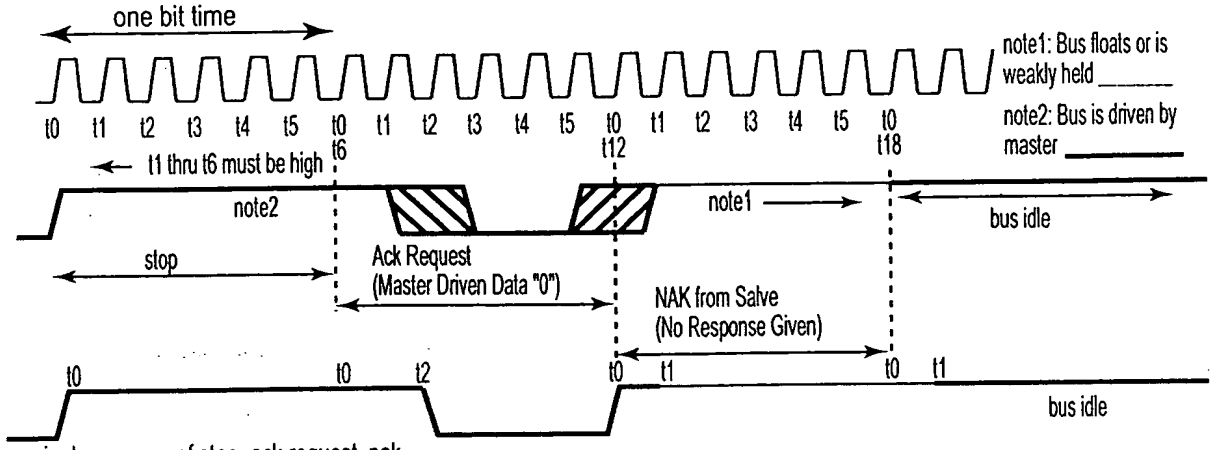


FIG. 19



Master Stop, Master Ack Req, Slave NAK

FIG. 20

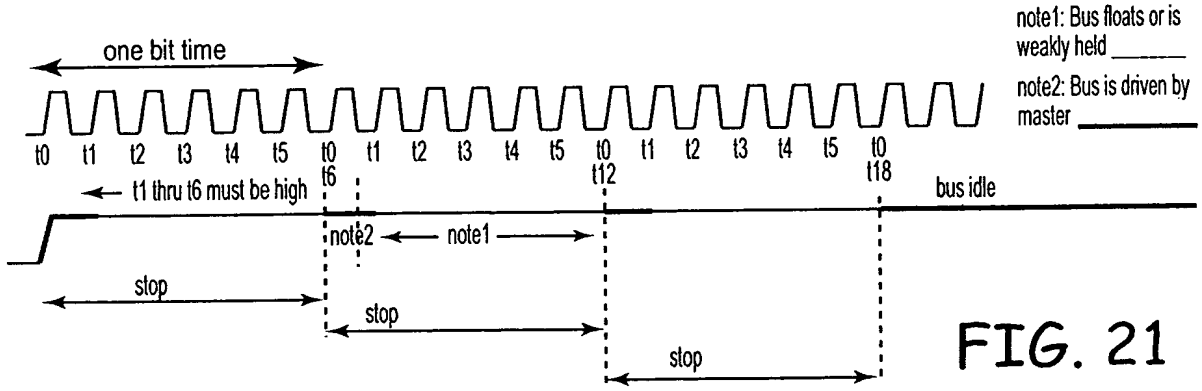
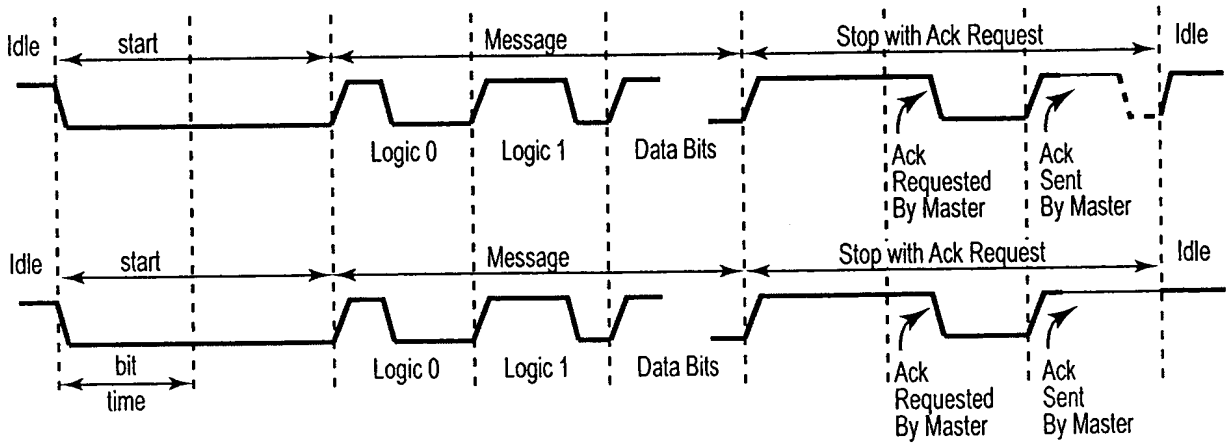


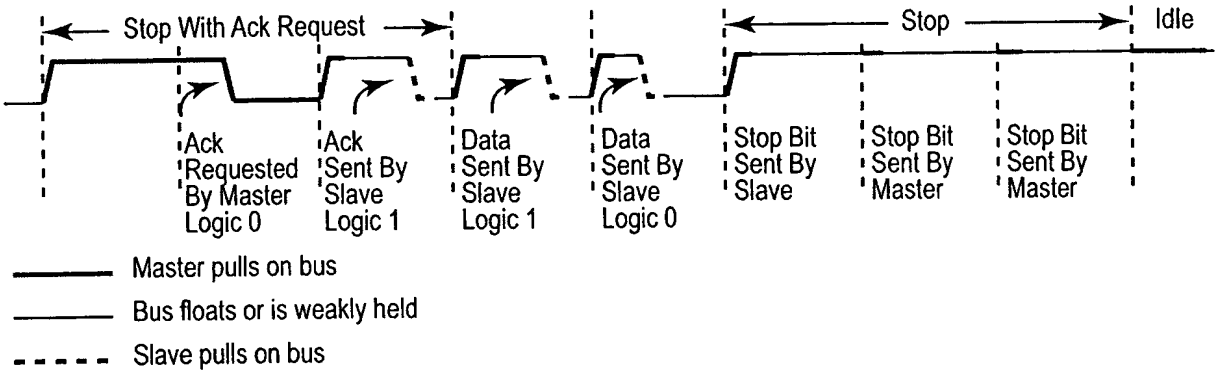
FIG. 21

Slave stop-stop-stop



Message from Master to One or more slaves

FIG. 22



A response with data from slave to master

FIG. 23

General Command Format

	msb...lsb						one bit	msb...lsb	msb...lsb	msb...lsb	Stop-AckReq-(N)Ack		
Master1	Master2						M3	Master4	Master5	Master6	Master7		Total Bit Times
Start	Slave(s)						QT	Master Command Name	Data	FCS	Stop Sequence		
2 bit times	6 bit times						1 bit time	5 bit times for most commands	8 bit times for most commands	8 bit times	3 bit times		33 for most Commands
	G_1	G_0	A_3	A_2	A_1	A_0							

FIG. 24

Long Address Format

64 bit Long Address					
msb...lsb	msb...lsb	msb...lsb	msb...lsb	msb...lsb	msb...lsb
6 Bit Manufacturer Code (up to 64 Manufacturers) 000000_2 = Medtronic 000012_2 = Viatron 000102_2 = MRG	6 bit Protocol Version (Each manufacturer) can have up to 64 different protocols)	21 bit Slave Model ID	20 bit Slave Serial Number (up to 1,048,576 unique slaves)	7 bit Manufacturing Facility (Manufacturer Specific) ACSII Char V = Medtronic Villalba Puerto Rico ASCIII Char R = Medtronic Rice Creek	4 bitt Slave Number (one lead could have 16 slaves) (allows numbering of the slaves on the lead)

FIG. 25

Slave Short Addresses and Multicast Examples

Slave Short Address	Master2					
	Slave(s)					
	G_1	G_0	A_3	A_2	A_1	A_0
0	0	0	0	0	0	1
1	0	0	0	0	1	0
2	0	0	0	1	0	0
3	0	0	1	0	0	0
4	0	1	0	0	0	1
5	0	1	0	0	1	0
6	0	1	0	1	0	0
7	0	1	1	0	0	0
8	1	0	0	0	0	1
9	1	0	0	0	1	0
A	1	0	0	1	0	0
B	1	0	1	0	0	0
C	1	1	0	0	0	1
D	1	1	0	0	1	0
E	1	1	0	1	0	0
F	1	1	1	0	0	0
Broadcast All	0	0	0	0	0	0
Multicast Slaves: 3.2.1.0	0	0	1	1	1	1
Multicast Slaves: 7.5.4	0	1	1	0	1	1
Multicast Slaves: B.A.8	1	0	1	1	0	1
Multicast Slaves: E.D.C	1	1	0	1	1	1

FIG. 26

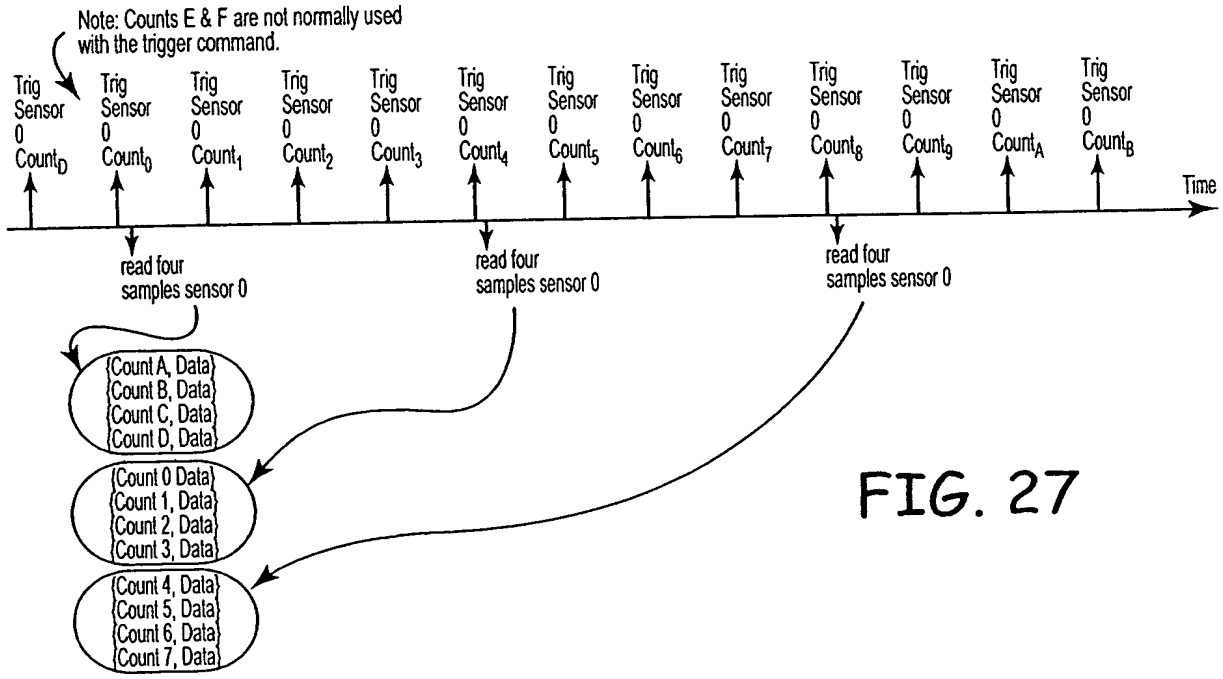


FIG. 27

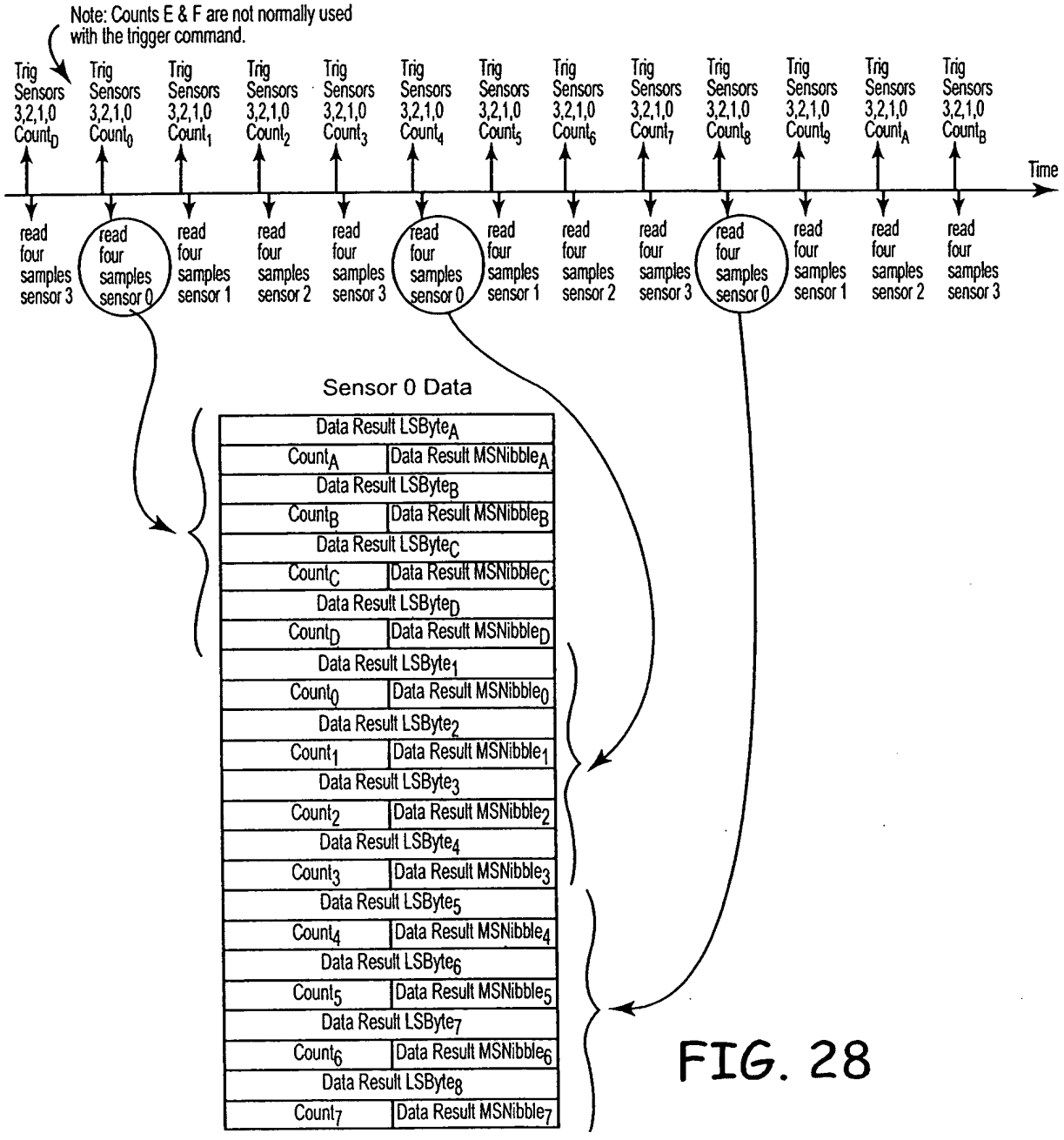

Note: Counts E & F are not normally used with the trigger command.
Trig Sensors 3,2,1,0 Count$_D$
Trig Sensors 3,2,1,0 Count$_0$
Trig Sensors 3,2,1,0 Count$_1$
Trig Sensors 3,2,1,0 Count$_2$
Trig Sensors 3,2,1,0 Count$_3$
Trig Sensors 3,2,1,0 Count$_4$
Trig Sensors 3,2,1,0 Count$_5$
Trig Sensors 3,2,1,0 Count$_6$
Trig Sensors 3,2,1,0 Count$_7$
Trig Sensors 3,2,1,0 Count$_8$
Trig Sensors 3,2,1,0 Count$_9$
Trig Sensors 3,2,1,0 Count$_A$
Trig Sensors 3,2,1,0 Count$_B$
Time
read four samples sensor 3
read four samples sensor 0
read four samples sensor 1
read four samples sensor 2
read four samples sensor 3
read four samples sensor 0
read four samples sensor 1
read four samples sensor 2
read four samples sensor 3
read four samples sensor 0
read four samples sensor 1
read four samples sensor 2
read four samples sensor 3
Sensor 0 Data
Data Result LSByte$_A$
Count$_A$ | Data Result MSNibble$_A$
Data Result LSByte$_B$
Count$_B$ | Data Result MSNibble$_B$
Data Result LSByte$_C$
Count$_C$ | Data Result MSNibble$_C$
Data Result LSByte$_D$
Count$_D$ | Data Result MSNibble$_D$
Data Result LSByte$_1$
Count$_0$ | Data Result MSNibble$_0$
Data Result LSByte$_2$
Count$_1$ | Data Result MSNibble$_1$
Data Result LSByte$_3$
Count$_2$ | Data Result MSNibble$_2$
Data Result LSByte$_4$
Count$_3$ | Data Result MSNibble$_3$
Data Result LSByte$_5$
Count$_4$ | Data Result MSNibble$_4$
Data Result LSByte$_6$
Count$_5$ | Data Result MSNibble$_5$
Data Result LSByte$_7$
Count$_6$ | Data Result MSNibble$_6$
Data Result LSByte$_8$
Count$_7$ | Data Result MSNibble$_7$

FIG. 28

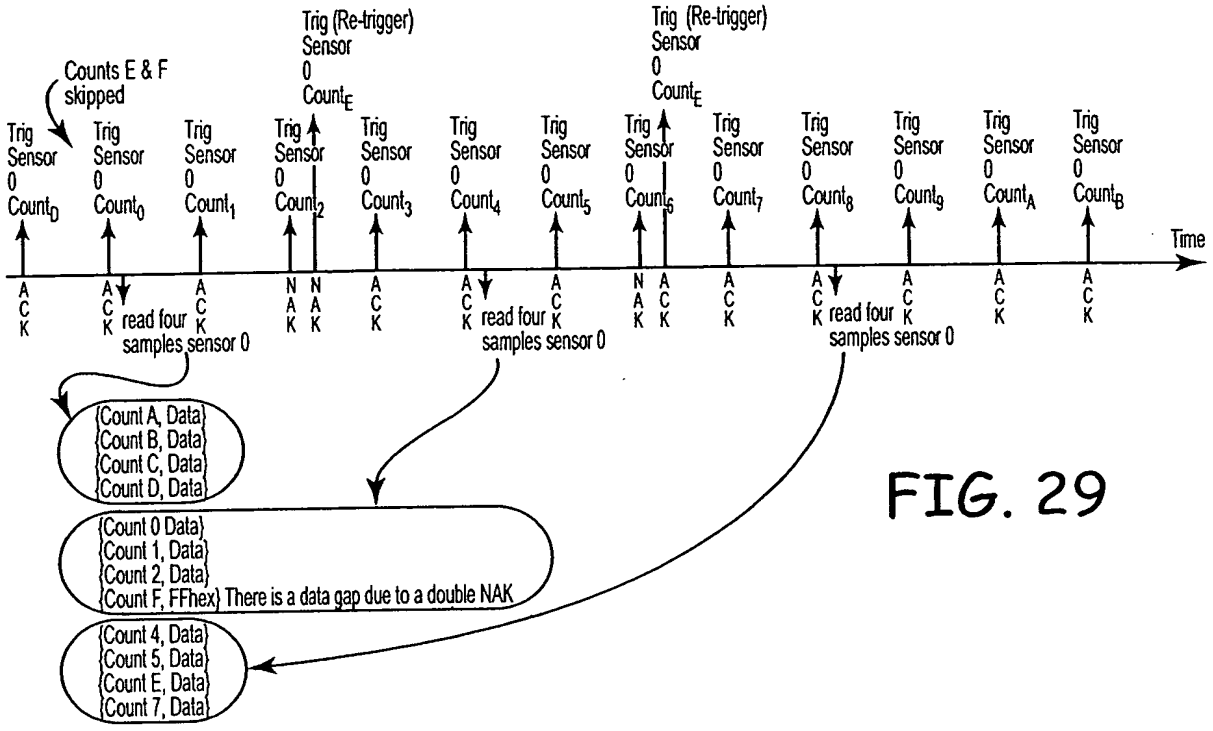

Counts E & F skipped
Trig (Re-trigger) Sensor 0 Count$_E$
Trig (Re-trigger) Sensor 0 Count$_E$
Trig Sensor 0 Count$_D$
Trig Sensor 0 Count$_0$
Trig Sensor 0 Count$_1$
Trig Sensor 0 Count$_2$
Trig Sensor 0 Count$_3$
Trig Sensor 0 Count$_4$
Trig Sensor 0 Count$_5$
Trig Sensor 0 Count$_6$
Trig Sensor 0 Count$_7$
Trig Sensor 0 Count$_8$
Trig Sensor 0 Count$_9$
Trig Sensor 0 Count$_A$
Trig Sensor 0 Count$_B$
Time
ACK
NAK
read four samples sensor 0
read four samples sensor 0
read four samples sensor 0
{Count A, Data}
{Count B, Data}
{Count C, Data}
{Count D, Data}
{Count 0 Data}
{Count 1, Data}
{Count 2, Data}
{Count F, FFhex} There is a data gap due to a double NAK
{Count 4, Data}
{Count 5, Data}
{Count E, Data}
{Count 7, Data}

FIG. 29

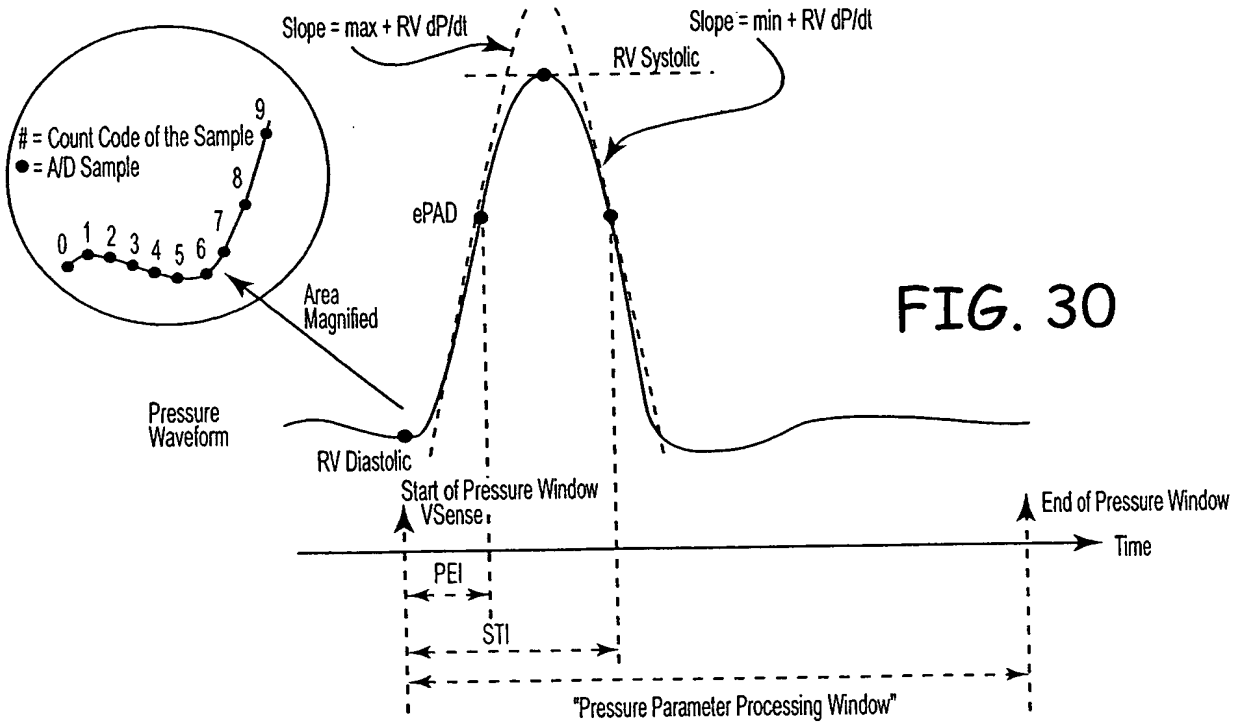

Slope = max + RV dP/dt
Slope = min + RV dP/dt
RV Systolic
= Count Code of the Sample
● = A/D Sample
0 1 2 3 4 5 6 7 8 9
ePAD
Area Magnified
Pressure Waveform
RV Diastolic
Start of Pressure Window
VSense
End of Pressure Window
Time
PEI
STI
"Pressure Parameter Processing Window"

FIG. 30

Command Codes and Measured Parameters

Command Codes	Measured Parameter	Description
Vsense		Command Code that is passed with a trigger down to the Defines the start of the "Pressure Parameter Processing Window".
End of Pressure Window		Command Code that is passed with a trigger down to the sensor. Defines the end of the "Pressure Parameter Processing Window".
	max + RV dP / dt	Maximum Positive dP/dt within "Pressure Parameter Processing Window".
	min. - RV dP / dt	Minimum Negative dP/dt within "Pressure Parameter Processing Window".
	PEI	Pre-Ejection Interval. Time interval from Vsense Command Code to + RV dP / dt point. Calculated from time stamp deltas of triggers.
	STI	Systolic Time Interval - Time interval from Vsense Command code to - RV dP dt point. Calculated from time stamp deltas of triggers.
	RV Systolic Pressure	Maximum Pressure. Systole is when the heart is squeezing to pump blood.
	RV Diastolic Pressure	Ideally Minimum Pressure but will be defined as pressure measured at Vsense trigger Command Code. Diastole is when the heart is relaxed and is filling with blood.
	RV Pulse Pressure	RV Systolic - RV Diastolic.
	ePAD	Pressure at max + RV dP/dt. ePAD is estimated Pulmonary Artery Diastolic pressure and gives an estimate of a snapshot of left ventricular pressure since the mitral valve is open at this point in time.

FIG. 31

Command Overview

Master Command Name	Command Length Bit Times	Command Usage
Unlocks (00hex)	33	Safety command for master to unlock/lock certain areas of memory or to unmap slaves so they only respond to the long addresses.
Search Long Address (01hex)	26-89 (As search progresses more and more of the long address is added onto the command)	Sends a string of bit(s) representing the long address stretching from MSB towards LSB. If a slave is at that long address and is unmapped then it pulls the DATA line low (i.e. does an ack).
Write Short Address (02hex)	89	Using the long address it assigns a short address
Trigger (03hex)	33	Triggering slaves. Each trigger has an associated Count and Command Code.
Quick Trigger (QT bit Set)	24	Triggering slaves with a command fewer bit time. Each trigger has an associated Count.
Read (04hex)	24 plus data response	Reads RAM/ Register Memory
Read Results (05hex)	33 plus data response	Reads Result (ADC) data out of RAM/Register Memory and has an automatic clear data function and resetting of pointer movement.
Write (06hex)	33	Writes a value into RAM/Register Memory
LSB RAM/REG Address (07hex)	33	Sets LSB portion of Pointer to RAM/Register Address Space
MSB RAM/REG Address (08hex)	33	Sets MSB portion of Pointer to RAM/Register Address Space
LSB EEPROM Address (09hex)	33	Sets LSB portion of Pointer to EEPROM Address Space
MSB EEPROM Address (0Ahex)	33	Sets MSB portion of Pointer to EEPROM Address Space
Copy RAM/REG to EEPROM memory (0Bhex)	33	Copies data from RAM/Register Address Space to EEPROM.
Copy EEPROM to RAM/REG memory (0Chex)	33	Copies data from EEPROM to RAM/Register address space.
Quick read (0Dhex)	33 plus data response	Reads the address pointers for debug. Reads the status by the error code and power monitoring.
Master Command Names OEhex thru 1Fhex are unused.		

FIG. 32

Master's Unlocks (00hex) Command

Master	Master2	M3	Master4	Master5		Master6	Master7	Total Bit Times
Start	Slaves Unicast or Broadcast See Table 16	QT	Master Commnad Name-Unlocks (00hex)	Unlock Key Code	Unlock Key Option	FCS	Stop-AckReq-(N)Ack	
2	6	1	5	5	3	8	3	33
	G_1 G_0 A_3 A_2 A_1 A_0	0						
		If Broadcast then all slaves (mapped or unmapped) listen to this command.						
		If Unicast and not for this slave then go to sleep after Master2.						

FIG. 33

Unlock Key Options

Master	M3	Master4	Master5		Explanation	Notes
Slave(s)	QT	Unlocks	Unlock Key Code(1)	Unlock Key Options		
Broadcast Only	0	(00hex)	00111_2 (07hex)	000_2 - Disallow writing a slave long address (and clock/supply trim) 111_2 - Allow writing a slave long address (and clock/supply trim)	Allows/Disallows setting the memory pointer via the LSB RAM/REG Address (07hex) and MSB RAM/REG Address (08hex) commands to those memory locations that contain the long address (and clock/supply trim) in volatile memory you need to unlock that ability with the copy commands (see below in this table)	(2)
Broadcast Only	0		00001_2 (01hex)	000_2 - Check for unmapped 001_2 - Check for mapped 111_2 - Unmap all slaves	Works in conjunction with the Search Long Address (01hex) command If 000_2 - is sent: "Check for unmapped" any unmapped slave will have an ACK response. If 001_2 - is sent: "Check for mapped" any mapped slave will have an ACK response.	(3)
Unicast Only	0		01011_2 (0Bhex)	000_2 - Disallow copying 111_2 - Allow copying	Works in conjunction with the Copy RAM/REG to EEPROM memory (0Bhex)	(4)
Unicast Only	0		01100_2 (0Chex)	000_2 - Disallow copying 111_2 - Allow copying	Works in conjunction with the Copy EEPROM to RAM/REG memory (0Chex)	(5)

FIG. 34

Master's Unlocks (00hex) Command

Master1	Master2	M3	Master4	Master5	Master6	Master7	Total Bit Times
Start	Slaves Broadcast	QT	Master Command Name Search Long Address (01hex)	Long Address	FCS	Stop Ackreq (N) Ack	
2	6	1	5	1 to 64 bits	8	3	26 to 89
	G_1 G_0 A_3 A_2 A_1 A_0	0					
				All slaves listen to this command whether mapped or unmapped since this command is Broadcast any slave that is mapped does not acknowledge this command see Table 18 (Example Search). A mapped slave may optionally go to sleep after filed Master 4.			

FIG. 35

Example Search

Step	Slave Long Address Bit Patter (Field Master4) (MSB first)	Slave 1010 response	Slave 1001 response	Found Slave
0	Send out an Unlocks (00hex) command forcing all the slaves to be unmapped. Skip this step if you are just checking for new slaves added.			
1	Send out an Unlocks (00hex) command checking for any unmapped slaves. The command is ACK'd since Slaves 1010 and 1001 will say they are unmapped.			
2	1	ack	ack	
3	11	nak	nak	
4	10	ack	ack	
5	101	ack	nak	
6	1011	nak	nak	
7	1010	ack	nak	1010
8	Send out a Write Short Address (02hex) command to assign 1010 a short address. This will make this slave mapped.			
9	Send out and Unlocks (00hex) command checking for any unmapped slaves. The command is ACK'd since Slave 1001 will say it is unmapped.			
10	1	nak (mapped)	ack	
11	11	nak (mapped)	nak	
12	10	nak (mapped)	ack	
13	101	nak (mapped)	nak	
14	100	nak (mapped)	nak	
15	1001	nak (mapped)	ack	1001
16	Send out a Write Short Address (02hex) command to assign 1001 a short address. This will make this slave mapped.			
17	Send out and Unlocks (00hex) command checking for any unmapped slaves. The command is NAK'd since both slaves 1010 and 1001 are mapped. This tells the master the search for unmapped slaves is completed.			

FIG. 36

Master's Write Short Address (02hex) Command

Master1	Master2	M3	Master4	Master5	Master6	Master7	Total Bit Times
Start	Slaves Unicast	QT	Master Command Name Write Short Address (02hex)	Long Address	FCS	Stop-Ackreq-(N) Ack	
2	6	1	5	64	8	3	89
	G_1 G_0 A_3 A_2 A_1 A_0	0					
					unmapped Long Address not for this above goes to sleep after Master5		
		Mapped - not for this slave go to sleep after Master2					

FIG. 37

Trigger (03hex) Command

Master1	Master2	M3	Master4	Master5		Master7	Master6	Total Bit Times
Start	Slave(s) Multicast	QT	Master Command Name-Trigger (o3hex)	Count	Command Code	Stop-AckREq-(N)Ac	FCS	
2	6	1	5	4	4	3	8	33
	G_1 G_0 A_3 A_2 A_1 A_0	0						
				unmapped - goes to sleep after Master4				
		Mapped - not for this slave go to sleep after Master2						

FIG. 38

Trigger Command Code for cardiac IMD

Trigger Command Code	Code Meaning
0000	RV Pace
0001	RV Sense
0010	RA Pace
0011	RA Sense
0100	LV Pace
0101	LV Sense
0110	LA Pace
0111	LA Sense
1000	unused
1001	unused
...	unused...
1110	no specific Command Code occurring
1111	Cleared Data

FIG. 39

Trigger Command Code for Sonomicrometry

Trigger Command Code	Code Meaning
0000	all listen external acoustic ping
0001	acoustic ping 0 listen 1,2,3,4
0010	acoustic ping 1 listen 0,2,3,4
0011	acoustic ping 2 listen 0,1,3,4
0100	acoustic ping 3 listen 0,1,2,4
0101	acoustic ping 4 listen 0,1,2,3
0110	TBD or error or unused do nothing
0111	TBD or error or unused do nothing
...	TBD or error or unused do nothing
1110	no specific Command Code occurring -don't reconfigure
1111	Cleared Data

FIG. 40

Quick Trigger (QT bit Set) Command

Master1	Master2	M3	Master4	Master5	Master6	Total Bit Times
Start	Slaves	QT	Count	FCS	Stop-AckReq-(N)Ack	
2	6	1	4	8	3	24
	G_1 G_0 A_3 A_2 A_1 A_0	1				
			unmapped - goes to sleep after Master3			
		Mapped - not for this slave go to sleep after Master2				

FIG. 41

Master's Write Short Address (02hex) Command

Master1	Master2	M3	Master4	Master5	Master6	Master7	Total Bit Times
Start	Slaves Unicast	QT	Master Command Name Read (04hex)	Quantity of bytes 1	FCS	Stop-Ackreq-(N) Ack (Slave Ack Master)	
2	6	1	5	8	8	3	24
	G_1 G_0 A_3 A_2 A_1 A_0	0					
				unmapped - goes to sleep after Master4			
		Mapped - not for this slave go to sleep after Master2					

FIG. 42

Slave's Read (04hex) Response

msb...lsb	msb...lsb	msb...lsb	msb...lsb	msb...lsb	msb...lsb	msb...lsb
Slave 0	Slave 1	Slave...	Slave x-3	Slave x-2	Slave x-1	Slave x
Data	Data	Data...	Data	Data	FCS	Stop-Stop-Stop
byte 0	byte 1	(multiple bytes)	byte n-2	byte n-1		

FIG. 43

Rules for Read Results (05hex) command

	Read Results (05hex) command is told to read Buffer 0	Read Results (05hex) command is told to read Buffer 1
If ADC Pointer is currently set to write to Buffer 0	1. Set Buffer 1's Count and/or Command Codes to F_{16} codes and have ADC point to top of Buffer 1. Data Result Values of Buffer 1 may or may not be cleared to F codes - this is slave dependent since may want to leave alone to save power. 2. Set Read Result Pointer to Top of Buffer 0. 3. Send up contents of Buffer 0 for quantity of bytes requested.	(Must be a retry re-read of Buffer 0) 1. Continue ADC writing Buffer 0 2. Set Read Result Pointer Top of Buffer 1. 3. Send up contents of Buffer 1 for quantity of bytes requested.
If ADC Pointer is currently set to write to Buffer 1	(Must be a retry re-read of Buffer 0) 1. Continue ADC writing Buffer 1. 2. Set Read Result Pointer Top of Buffer 0. 3. Send up contents of Buffer 0 for quantity of bytes requested.	1. Set Buffer 0's Count and/or Command Codes to F_{16} codes and have ADC point to top of Buffer 0. Data Result Values of Buffer 0 may or may not be cleared to F codes - this is slave dependent since may want to leave alone to save power. 2. Set Read Result Pointer to Top of Buffer 1. 3. Send up contents of Buffer 1for quantity of bytes requested.

FIG. 44

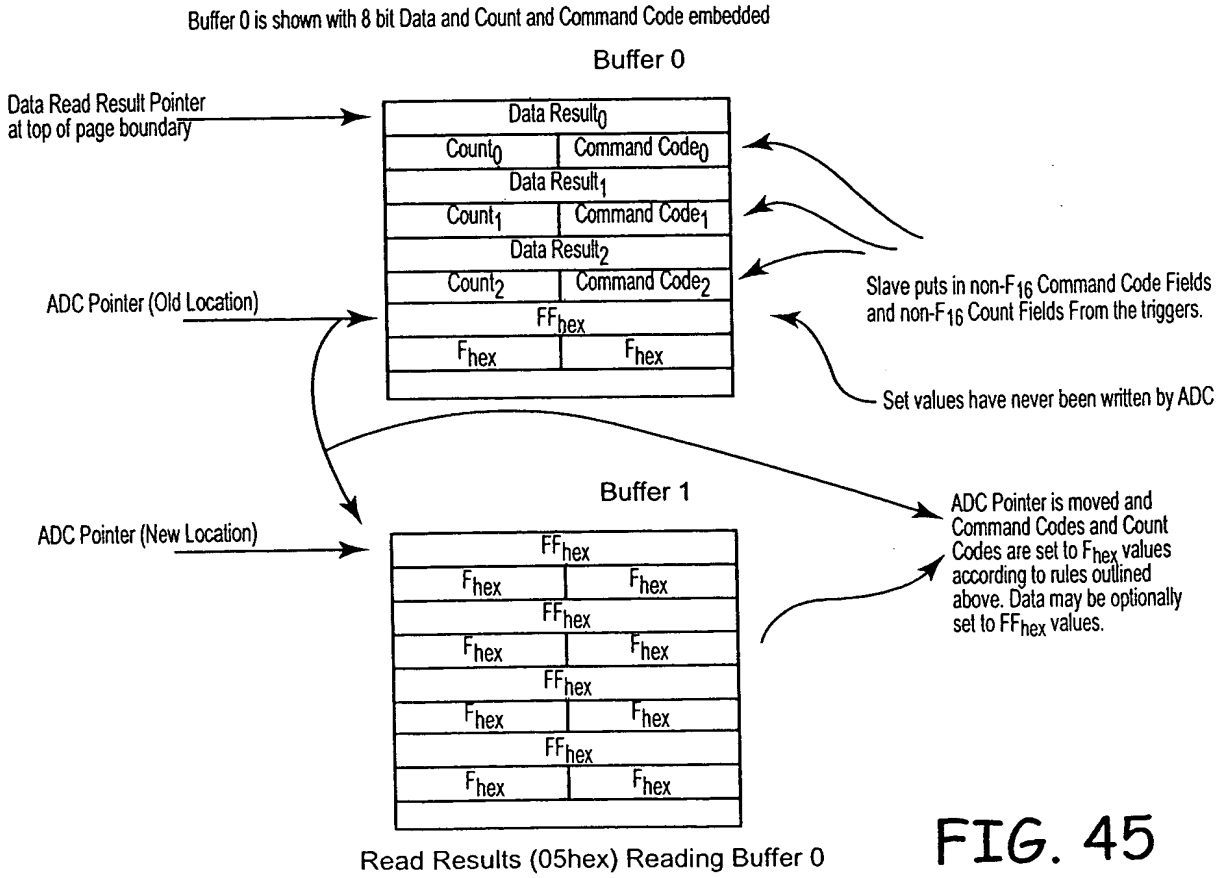


FIG. 45

Master's Road Results (05hex) Command

Master1	Master2	M3	Master4	Master5		M6	Master7	Total Bit Times
Start	Slave	QT	More Command Name -	Buffer	Quantity of	FCS	Stop-AckREq-(N)Ack	
2	6	1	5	1	7	8	3	33
	G_1 G_0 A_3 A_2 A_1 A_0	1						
				unmapped - goes to sleep after Master4				
		Mapped - not for this slave go to sleep after Master2						

FIG. 46

Slave's Read Results (05hex) Example Response

msb...lsb	msb...lsb	msb...lsb	msb...lsb	msb...lsb	msb...lsb	msb...lsb	msb...lsb	
Slave 1	Slave 2		Slave...	Slave x-3	Slave x-2		Slave x-1	Slave x
$Data_0$	$Count_0$	Command $Code_0$	(multiple bytes)...	$Data_n$	$Count_n$	Command $Code_n$	FCS	Stop-Stop-Stop

FIG. 47

Master's Write (06hex) Command

Master1	Master2	M3	Master4	Master5	M6	Master7	Total Bit Times
Start	Slave Unicast Preferred (Acknowledge will have value)	QT	Master Command Name- White (06hex)	Value Byte to write	FCS	Stop-AckREq-(N)Ack (slave ACK master)	
2	6	1	5	8	8	3	33
	G_1 G_0 A_3 A_2 A_1 A_0	0					
				unmapped - goes to sleep after Master4			
		Mapped - not for this slave go to sleep after Master2					

FIG. 48

Master's LSB RAM/REG Address (07hex) Command

Master1	Master2	M3	Master4	Master5	M6	Master7	Total Bit Times
Start	Slave Unicast Preferred (Acknowledge will then have value)	QT	Master Command Name- LSB RAM/REG Address (07hex)	LSB Value	FCS	Stop-AckREq-(N)Ack (slave ACK master)	
2	6	1	5	8	8	3	33
	G_1 G_0 A_3 A_2 A_1 A_0	0					
				unmapped - goes to sleep after Master4			
		Mapped - not for this slave go to sleep after Master2					

FIG. 49

Master's MSB RAM/REG Address (08hex) Command

Master1	Master2	M3	Master4	Master5	M6	Master7	Total Bit Times
Start	Slave Unicast Preferred (Acknowledge will have value)	QT	Master Command Name-MSB RAM/REG Address (08hex)	MSB Value Byte to write	FCS	Stop-AckREq-(N)Ack	
2	6	1	5	8	8	3	33
	G_1 G_0 A_3 A_2 A_1 A_0	0					
				unmapped - goes to sleep after Master4			
		Mapped - not for this slave go to sleep after Master2					

FIG. 50

Master's LSB EEPROM Address (09hex) Command

Master1	Master2	M3	Master4	Master5	M6	Master7	Total Bit Times
Start	Slave Unicast Preferred (Acknowledge will then have value)	QT	Master Command Name-LSB EEPROM Address (09hex)	LSB Value	FCS	Stop-AckREq-(N)Ack	
2	6	1	5	8	8	3	33
	G_1 G_0 A_3 A_2 A_1 A_0	0					
				unmapped - goes to sleep after Master4			
		Mapped - not for this slave go to sleep after Master2					

FIG. 51

Master's MSB EEPROM Address (0Ahex) Command

Master1	Master2	M3	Master4	Master5	M6	Master7	Total Bit Times
Start	Slave Unicast Preferred (Acknowledge will then have value)	QT	Master Command Name-MSB EEPROM Address (0Ahex)	MSB Value	FCS	Stop-AckREq-(N)Ack	
2	6	1	5	8	8	3	33
	G_1 G_0 A_3 A_2 A_1 A_0	0					
				unmapped - goes to sleep after Master4			
		Mapped - not for this slave go to sleep after Master2					

FIG. 52

Master's copy RAM/REG to EEPROM memory (0Bhex) Command

Master1	Master2	M3	Master4	Master5	M6	Master7	Total Bit Times
Start	Slave Unicast Preferred (Acknowledge will then have value)	QT	Master Command Name-Copy RAM/REG to EEPROM memory (0Bhex)	Quantity of Bytes 1	FCS	Stop-AckREq-(N)Ack	
2	6	1	5	8	8	3	33
	G_1 G_0 A_3 A_2 A_1 A_0	0					
				unmapped - goes to sleep after Master4			
		Mapped - not for this slave go to sleep after Master2					

FIG. 53

Master's copy to EEPROM to RAM/REG Memory (0Chex) Command

Master1	Master2	M3	Master4	Master5	M6	Master7	Total Bit Times
Start	Slave Unicast Preferred (Acknowledge will then have value)	QT	Master Command Name-Copy to EEPROM to RAM/REG memory (0Chex)	Quantity of Bytes-1	FCS	Stop-AckREq-(N)Ack	
2	6	1	5	8	8	3	33
	G_1 G_0 A_3 A_2 A_1 A_0	0					
				unmapped - goes to sleep after Master4			
		Mapped - not for this slave go to sleep after Master2					

FIG. 54

Master's Quick Read (oDhex) Command

Master1	Master2	M3	Master4	Master5	M6	Master7	Total Bit Times
Start	Slave Unicast	QT	Master Command Name-Quick Read (0Dhex)	QRAddress	FCS	Stop-AckREq-(N)Ack	
2	6	1	5	8	8	3	33
	G_1 G_0 A_3 A_2 A_1 A_0	0					
				unmapped - goes to sleep after Master4			
		Mapped - not for this slave go to sleep after Master2					

FIG. 55

Master's Which Pointer to Read

Master5	Description of what it points to
QRAddress	
00_{16}	EEPROM Address Pointer
01_{16}	RAM Register Space Address Pointer
02_{16}	ADC Address Buffer Pointer
03_{16}	Status Word

FIG. 56

Slave's Quick Read (0Dhex) Response

msb...lasb	msb...lasb	msb...lasb	msb...lasb
Slave 1	Slave 2	Slave 3	Slave 4
Data	Data	FCS	Stop-Stop-Stop
MSB	LSB		

FIG. 57

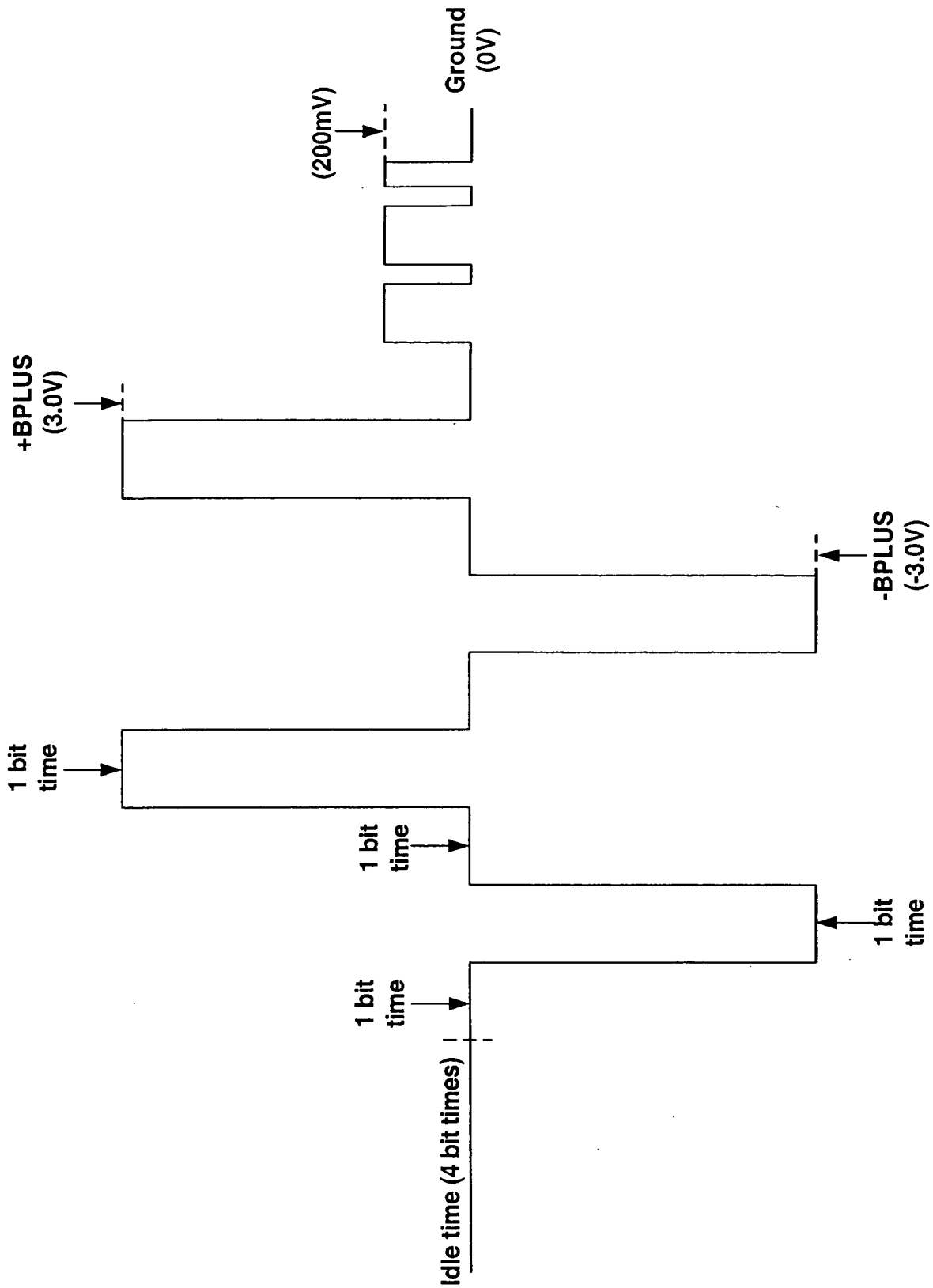


FIG. 58

Power and data pulses on two-wire bus

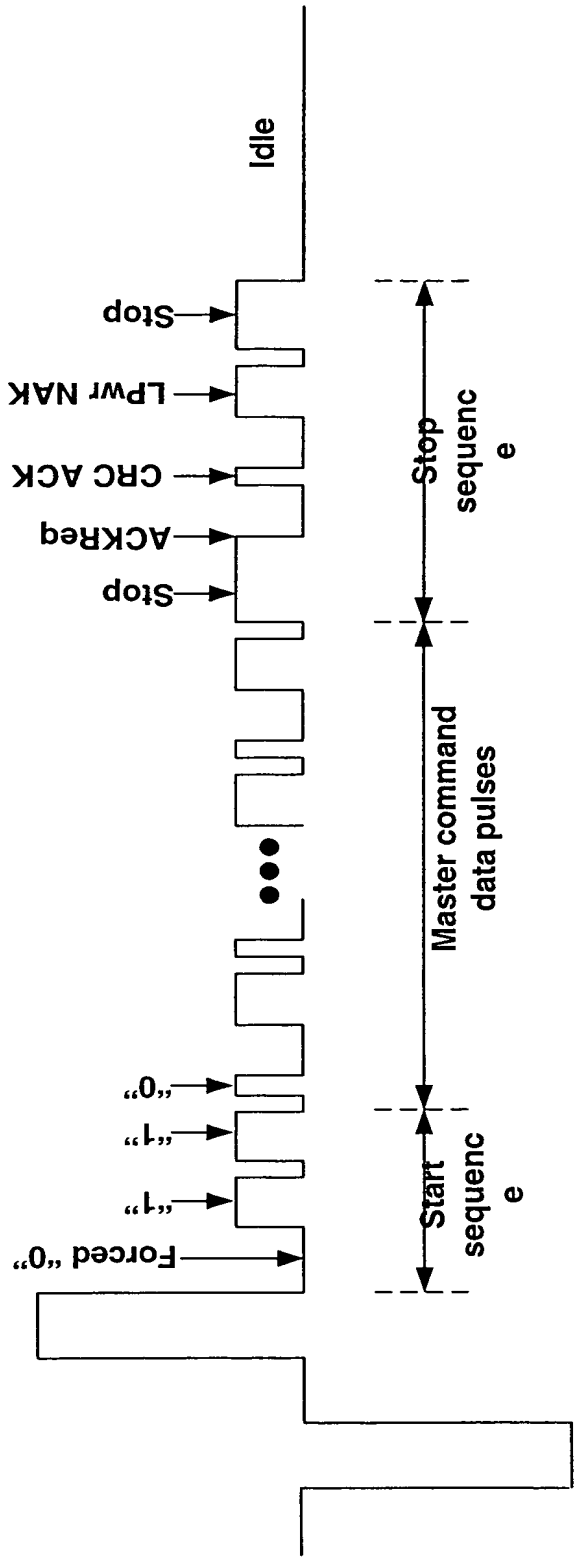


FIG. 59

Example of power and data sequence with Start and Stop sequences

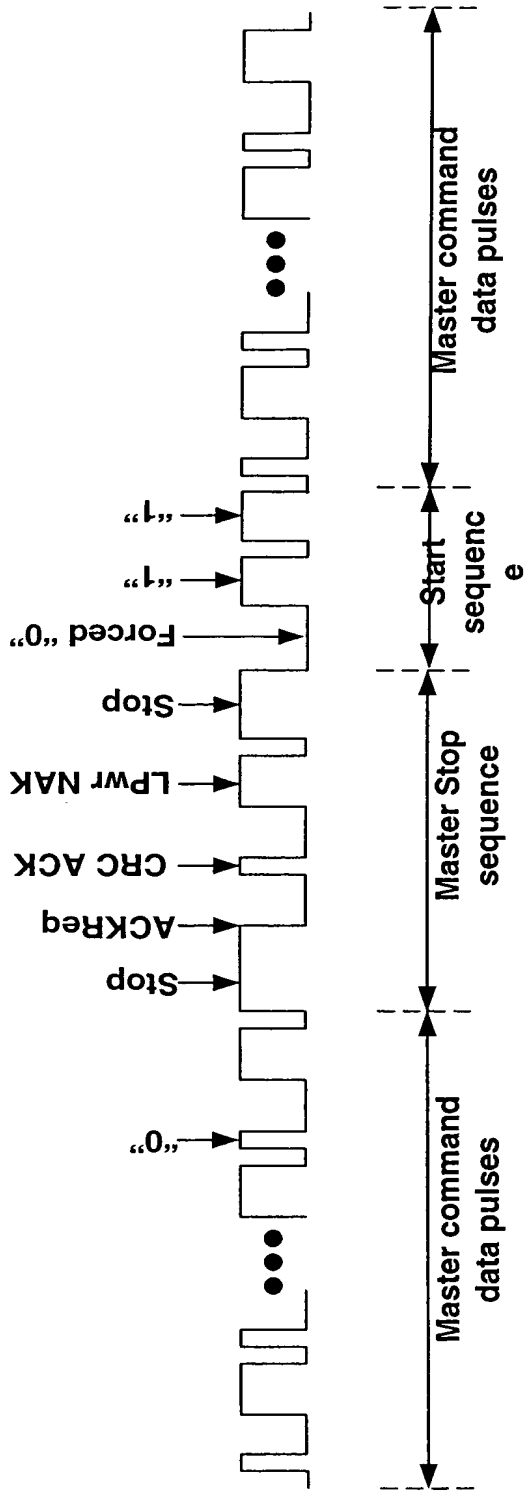


FIG. 60

Example of streaming messages